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John T. Peoples 14 Blue Jay Court Warren, NJ 07059			ART UNIT	PAPER NUMBER
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DATE MAILED: 04/04/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/882,075

Applicant(s) **AK**

LI, SHUO-YEN ROBERT

Examiner

Tri H. Phan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 12-21 and 25 is/are rejected.
- 7) ☐ Claim(s) 9-11 and 22-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/15/2001</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is in response to the Response/Amendment filed on May 28<sup>th</sup>, 2002.

New claim 25 is added. Claims 1-25 are now pending in the application.

### ***Specification***

2. The disclosure is objected to because of the following informalities:

In page 13, line 15, FIG. "28A" is a typographical error; it should be correct to -- 28B --.

In page 14, line 12, FIGS. "33A-D" is a typographical error; it should be correct to -- 33A-F --.

In page 17, line 16, the brief description of the FIGS. 56A-D is missing.

Appropriate corrections are required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

4. Claims 1-3, 5-7, 9-12, 15-17 and 19-25 are objected to because of the following informalities:

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In claim 1, it recites limitations such as “ $2^n$ ”, “ $b_1, b_2, \dots, b_n$ ”, “ $\gamma(k)$ ”; wherein the recitations “ $n$ ” and “ $k$ ” are not defined and leave open-ended; it should be defined in the claim for clearly setting forth the metes and bounds of the patent protection desired. Similar problems exist in claims 2, 3, 5-7, 9-12, 15-17 and 19-24.

In claim 9, it recites limitations such as “ $2^r$ ”, “ $r$ ”, “ $p_1 \dots p_r$ ”, “ $Q_{\gamma(1)} p_1 \dots p_r Q_{\gamma(2)} \dots Q_{\gamma(k)}$ ”; wherein the recitations “ $r$ ” leave open-ended and “ $k$ ” are not defined and leave open-ended; it should be defined in the claim for clearly setting forth the metes and bounds of the patent protection desired. Similar problems exist in claims 11, 16, and 22-24.

In claim 25, it recites the limitation such as “ $p$ ”, “ $q$ ”; which are not defined and leave open-ended; it should be defined in the claim for clearly setting forth the metes and bounds of the patent protection desired.

In claim 1, the limitations “the routing tag” (line 11), “the  $j$ -th stage cell” (line 14) should be correct to -- a routing tag --; -- a  $j$ -th stage cell --; for clarity.

In claim 2, the limitation “the  $j$ -th stage cell” (line 14) should be correct to -- a  $j$ -th stage cell -- for clarity. Same objection with claim 3, for the limitations “the  $j$ -th stage cell” (line 15).

In claim 8, the limitation “the tiebreaker” (line 5) should be correct to -- a tiebreaker --; for clarity. Same objection with claim 16, line 5; claim 22, line 5, for the limitations “the tiebreaker”.

Appropriate corrections are required.

***Double Patenting***

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5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-7, 12-15, and 17-21, are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 09/882,005 (hereinafter '005'). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

For claims 1, 3-7, and 12-15, the claimed inventions 1-15 of '005' disclose the method for self-routing a packet through a  $2^n \times 2^n$  switch, the switch having  $2^n$  external output ports labeled with  $2^n$  distinct binary output addresses in the form of  $b_1, b_2, \dots, b_n$ , and is composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide  $\gamma(1), \gamma(2), \dots, \gamma(k)$  where  $\gamma$  is a mapping from the set  $\{1, 2, \dots, k\}$  to the set  $\{1, 2, \dots, n\}$ , wherein each of the switching cells is a sorting cell associated with the partial order " $0$  (0-bound)  $< 1$  (1-bound)", the packet being destined for a binary output address  $d_1, d_2, \dots, d_n$ , the method comprising generating a routing tag  $d_{\gamma(1)}d_{\gamma(2)} \dots d_{\gamma(k)}$  for the packet with reference to the guide and the destination output address of the packet, and routing the packet through the network by using  $d_{\gamma(j)}$  in the routing tag in the j-th

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stage cell,  $1 \leq j \leq k$ , to select an output from the  $j$ -th stage cell to emit the packet (see claims 1 and 6);

wherein generating a routing tag includes computing the guide transform of the destination address (see claim 2);

wherein the destination address is expressed as binary  $(d_1, d_2, \dots, d_k)$  and the guide transform is expressed as  $\gamma(1), \gamma(2), \dots, \gamma(k)$ , and wherein the computing includes generating binary  $(d_{\gamma(1)}d_{\gamma(2)} \dots d_{\gamma(k)})$  (see claim 3);

wherein the method including prepending binary  $d_{\gamma(1)}d_{\gamma(2)} \dots d_{\gamma(k)}$  to the packet (see claim 4).

wherein the network is an  $n$ -stage network composed of nodes, the guide transform is expressed as  $\gamma(1), \gamma(2), \dots, \gamma(n)$  and wherein, for an  $j$ -th stage node, the routing includes using  $d_{\gamma(j)}$  in the  $j$ -th stage node to select an output from the  $j$ -th stage node to emit the packet,  $1 \leq j \leq n$  (see claim 5);

wherein the routing includes removing the bit  $d_{\gamma(j)}$  from the routing tag before the packet exits the  $j$ -th stage cell,  $1 \leq j \leq k$  (see claim 7);

wherein the routing includes using the leading bit in the routing tag in the  $j$ -th stage cell,  $1 \leq j \leq k$ , to select an output from the  $j$ -th stage cell to emit the packet (see claim 8);

wherein the routing includes the removing the leading one bit from the routing tag of the packet before the packet exits the  $j$ -th stage cell,  $1 \leq j \leq k$  (see claim 9);

wherein the switch is characterized as an  $n$ -stage banyan-type network with guide  $\gamma(1), \gamma(2), \dots, \gamma(n)$ , where  $\gamma$  is a permutation on the integers from 1 to  $n$  (see claim 10);

wherein the packet is an idle packet which is a stream of '0' bits such that the packet is either a real data packet or an idle packet (see claim 11);

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wherein the sorting cell is associated with the partial order " $10$  ('**0-bound**')  $< 00$  ('**idle**')  $< 11$  ('**1-bound**')" (see claim 12);

wherein generating the routing tag includes generating the routing tag  $1d_{\gamma(1)}d_{\gamma(2)} \dots d_{\gamma(k)}$  for a real data packet (see claim 13);

wherein the routing includes using  $1d_{\gamma(j)}$  in the routing tag of the real data packet in the  $j$ -th stage cell,  $1 \leq j \leq k$ , to select an output from the  $j$ -th stage cell to emit the real data packet (see claim 14);

wherein the routing includes removing the bits  $1d_{\gamma(j)}$  from the routing tag before the real data packet exits from the  $j$ -th stage cell,  $1 \leq j \leq k$  (see claim 15).

For claims 2 and 17-21, the claimed inventions 16, and 7-12 of '005' disclose a  $2^n \times 2^n$  self-routing switch having an array of  $2^n$  external input ports and an array of  $2^n$  external output ports with  $2^n$  distinct binary output addresses in the form of  $b_1, b_2, \dots, b_n$ , for switching a packet, the packet being either a real data packet destined for an  $n$ -bit binary destination address, or being an idle packet having no pre-determined destination output address, the switch comprising

a switch fabric with external input ports, the switch fabric having a plurality of switching cells interconnected into a  $k$ -stage bit-permuting network which is characterized by the guide  $\gamma(1), \gamma(2), \dots, \gamma(k)$ , where  $\gamma$  is a mapping from the set  $\{1, 2, \dots, k\}$  to the set  $\{1, 2, \dots, n\}$ ,

a routing tag circuit, coupled to the external input ports, for generating a routing tag  $1d_{\gamma(1)}d_{\gamma(2)} \dots d_{\gamma(k)}$  for each of the real data packets with reference to the guide of the bit-permuting network and the destination output address of the packet, and

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a routing control circuit, coupled to the switching cells, for routing the real data packet through the switch by using  $1d_j(j)$  in the routing tag of the packet in the  $j$ -th stage cell,  $1 \leq j \leq k$ , to select an output from the  $j$ -th stage cell to emit the packet (see claim 16).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-8, 12-21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lee, Hee-choul** (U.S.6,335,930; hereinafter '**Lee**') in view of **Yang et al.** (U.S.5,940,389; hereinafter '**Yang**').

- In regard to claims 1 and 3, **Lee** discloses in Figs. 5-20 and in the respective portions of the specification about the method for self-routing a plurality of packets through a  $2^n \times 2^n$  switch ('multi-stage  $N \times N$  interconnection network'; For example see Fig. 6; Abstract), the switch having  $2^n$  external input ports ('input ports') and  $2^n$  external output ports ('output ports') labeled with  $2^n$  distinct binary output addresses in the form of  $b_1, b_2, \dots, b_n$ , and composed of a plurality of switching cells ('switching element') interconnected into a  $k$ -stage bit-permuting network



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(‘switching stage’; For example see Figs. 5-6; col. 8, line 25-49) which is characterized by the guide  $\gamma(1), \gamma(2), \dots, \gamma(k)$  where  $\gamma$  is a mapping from the set  $\{1, 2, \dots, k\}$  to the set  $\{1, 2, \dots, n\}$ , each of the packets destined for a rectangular set of output addresses represented by a quaternary sequence  $Q_1, Q_2, \dots, Q_n$ , the method generates a routing tag  $Q_{\gamma(1)}Q_{\gamma(2)} \dots Q_{\gamma(k)}$  for each of the packets with reference to the guide of the bit-permuting network and the destination output addresses of the packet (‘MRN generation logic’; For example see Fig. 13; col. 15, lines 53-58), and routes each of the packets through the network by using  $Q_{\gamma(j)}$  in the routing tag of the packet in the  $j$ -th stage cell,  $1 \leq j \leq k$ , to select an output or both outputs from the  $j$ -th stage cell to emit the packet (‘input port controller’ and ‘central priority arbitrator’; For example see Figs. 15-17; col. 16, lines 60-65; wherein the input port controller routes the packet to one of the output ports with the assistance of the central priority arbitrator). **Lee** does disclose about the  $Q_j$  is the quaternary symbol in any one of the three values: ‘0-bound’, ‘1-bound’, the other combinations such as ‘001’ to ‘110’, but fails to explicitly disclose about the ‘bicast’ value, wherein each of the switching cells is a sorting cell associated with the partial order (For example see Figs. 6-7; col. 8, line 58 through col. 9, line 30; col. 10, lines 9-15; wherein ‘000’, ‘111’ are ‘0-bound’, ‘1-bound’ values), but fails to explicitly disclose about the ‘bicast’ value. However, such implementation is known in the art.

For example, **Yang** discloses about the system and method for assigning routing tag for routing signals through the Benes network with input and output stages comprising  $2 \times 2$   $\beta$  elements (For example see Figs. 11-20; col. 10, lines 32-53); wherein the control circuit generates the routing tags and the comparator generates different control sequences such as ‘00’, ‘01’, ‘10’ and ‘11’ (For example see col. 10, line 40-53; wherein ‘00’ and ‘11’ are ‘0-bound’,

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**'1-bound'** values; and **'01'**, **'10'** are the **'bicast'** value) for each input signal (For example see col. 18, line 63 through col. 19, line 18) to support grouping channels, e.g. multicasting.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Yang**, by implementing the control circuit and routing tag generator, in assigning different control sequences for the routing tag, into the **Lee's** controller and arbitrator, with the motivation being to improve the ability to support grouping channels as disclosed in **Yang**: col. 9, lines 15-25.

- Regarding claims 4, 14, and 18, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), **Lee** further discloses wherein each quaternary symbol is coded by two bits, where the values **'0-bound'**, **'1-bound'** are coded as **'11'**, **'00'**, respectively (For example see Figs. 6-7; col. 8, line 58 through col. 9, line 30; col. 10, lines 9-15; wherein **'000'**, **'111'** are **'0-bound'**, **'1-bound'** values). but fails to explicitly disclose about the **'bicast'** value. However, such implementation is known in the art.

For example, **Yang** discloses about the **'idle'** and **'bicast'** coded as **'10'**, and **'01'** (For example see col. 10, line 40-53; wherein **'00'** and **'11'** are **'0-bound'**, **'1-bound'** values; and **'01'**, **'10'** are the **'idle'** and **'bicast'** values).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Yang**, by implementing the control circuit and routing tag generator, in assigning different control sequences such as **'00'**, **'01'**, **'10'** and **'11'** for the routing tag, into the **Lee's** controller and arbitrator, with the

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motivation being to improve the ability to support grouping channels as disclosed in **Yang**: col. 9, lines 15-25.

- In regard to claims 5-6 and 19-20, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), **Lee** further discloses about using the output module for removing the routing information attached to each packet to retransmit to the output ports ("*removing the quaternary symbol*"; For example see Fig. 13; col. 18, lines 21-31) based on the ternary number ("*quaternary symbol*").

- Regarding claims 7, 15, 21 and 25, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), **Lee** further discloses about the multistage omega network in performing self-routing by using the routing tag ("*n-stage banyan type network*"; For example see Fig. 6; col. 8, line 60 through col. 9, line 31).

- In regard to claim 8, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), **Lee** further discloses about the central priority arbitrator in generating routing tag ("*priority code*"; For example see Fig. 15, 17; col. 16, lines 60-65; col. 17, lines 50-54)

- Regarding claims 12, **Lee** discloses in Figs. 5-20 and in the respective portions of the specification about the method for self-routing a plurality of packets through a  $2^n \times 2^n$  switch ('multi-stage NxN interconnection network'; For example see Fig. 6; Abstract), the switch

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having  $2^n$  external input ports ('input ports') and  $2^n$  external output ports ('output ports') labeled with  $2^n$  distinct binary output addresses in the form of  $b_1, b_2, \dots, b_n$ , and composed of a plurality of switching cells ('switching element') interconnected into a k-stage bit-permuting network ('switching stage'; For example see Figs. 5-6; col. 8, line 25-49) which is characterized by the guide  $\gamma(1), \gamma(2), \dots, \gamma(k)$  where  $\gamma$  is a mapping from the set  $\{1, 2, \dots, k\}$  to the set  $\{1, 2, \dots, n\}$ , each of the packets destined for a rectangular set of output addresses represented by a quaternary sequence  $Q_1, Q_2, \dots, Q_n$ , the method generates a routing tag  $Q_{\gamma(1)}Q_{\gamma(2)} \dots Q_{\gamma(k)}$  for each of the packets with reference to the guide of the bit-permuting network and the destination output addresses of the packet ('MRN generation logic'; For example see Fig. 13; col. 15, lines 53-58), and routes each of the packets through the network by using  $Q_{\gamma(j)}$  in the routing tag of the packet in the j-th stage cell,  $1 \leq j \leq k$ , to select an output or both outputs from the j-th stage cell to emit the packet ('input port controller' and 'central priority arbitrator'; For example see Figs. 15-17; col. 16, lines 60-65; wherein the input port controller routes the packet to one of the output ports with the assistance of the central priority arbitrator). Lee does disclose about generating the idle packet ("*idle packet*"; For example see col. 16, line 20-24) the  $Q_j$  is the quaternary symbol in any one of the three values: '0-bound', '1-bound', the other combinations such as '001' to '110', but fails to explicitly disclose about the 'bicast' value, wherein each of the switching cells is a sorting cell associated with the partial order (For example see Figs. 6-7; col. 8, line 58 through col. 9, line 30; col. 10, lines 9-15; wherein '000', '111' are '0-bound', '1-bound' values), but fails to explicitly disclose about the 'bicast' value. However, such implementation is known in the art.

For example, **Yang** discloses about the system and method for assigning routing tag for routing signals through the Benes network with input and output stages comprising  $2 \times 2$   $\beta$  elements (For example see Figs. 11-20; col. 10, lines 32-53); wherein the control circuit generates the routing tags and the comparator generates different control sequences such as '00', '01', '10' and '11' (For example see col. 10, line 40-53; wherein '00' and '11' are '**0-bound**', '**1-bound**' values; and '01', '10' are the "idle" '**bicast**' value) for each input signal (For example see col. 18, line 63 through col. 19, line 18) to support grouping channels, e.g. multicasting.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Yang**, by implementing the control circuit and routing tag generator, in assigning different control sequences for the routing tag, into the **Lee**'s controller and arbitrator, with the motivation being to improve the ability to support grouping channels as disclosed in **Yang**: col. 9, lines 15-25.

- In regard to claims 2 and 17, **Lee** discloses in Figs. 5-20 and in the respective portions of the specification about the method for self-routing a plurality of packets through a  $2^n \times 2^n$  switch ('multi-stage  $N \times N$  interconnection network'; For example see Fig. 6; Abstract), which has the array of  $2^n$  external input ports ('input ports') and an array of  $2^n$  external output ports ('output ports') with  $2^n$  distinct binary output addresses in the form of  $b_1, b_2, \dots, b_n$  for routing a packet, the packet being either a real data packet destined for a rectangular set of output addresses represented by a quaternary sequence  $Q_1, Q_2, \dots, Q_n$ , where each  $Q_j$  is a quaternary symbol having one of the values of '**0-bound**', '**1-bound**' (For example see Figs. 5-6; col. 8, line 25 through col. 9, line 31), or being an idle packet having no pre-determined destination output

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address (“idle packet”; For example see col. 16, line 20-24), a switching fabric (For example see Figs. 5-6) having a plurality of switching cells (‘switching element’) interconnected into a k-stage bit-permuting network (‘switching stage’) which is characterized by the guide  $\gamma(1)$ ,  $\gamma(2)$ ,  $\dots$ ,  $\gamma(k)$ , where  $\gamma$  is a mapping from the set  $\{1, 2, \dots, k\}$  to the set  $\{1, 2, \dots, n\}$ , routing tag circuitry, coupled to the external input ports, for generating a routing tag  $Q_{\gamma(1)}Q_{\gamma(2)} \dots Q_{\gamma(k)}$  for the packet with reference to the guide of the bit-permuting network and the destination addresses of the packet (‘input port controller’ and ‘MRN generation logic’; For example see Fig. 13; col. 15, lines 53-58), and routing control circuitry, coupled to the switching cells, for routing the packet through the switch by using  $Q_{\gamma(j)}$  in the routing tag in the j-th stage cell,  $1 \leq j \leq k$ , to select an output or both outputs from the j-th stage cell to emit the packet (‘central priority arbitrator’; For example see Figs. 15-17; col. 16, lines 60-65). but fails to explicitly disclose about the ‘**bicast**’ value, wherein each of the switching cells is a sorting cell associated with the partial order (For example see Figs. 6-7; col. 8, line 58 through col. 9, line 30; col. 10, lines 9-15; wherein ‘000’, ‘111’ are ‘**0-bound**’, ‘**1-bound**’ values), but fails to explicitly disclose about the ‘**bicast**’ value. However, such implementation is known in the art.

For example, **Yang** discloses about the system and method for assigning routing tag for routing signals through the Benes network with input and output stages comprising  $2 \times 2$   $\beta$  elements (For example see Figs. 11-20; col. 10, lines 32-53); wherein the control circuit generates the routing tags and the comparator generates different control sequences such as ‘00’, ‘01’, ‘10’ and ‘11’ (For example see col. 10, line 40-53; wherein ‘00’ and ‘11’ are ‘**0-bound**’, ‘**1-bound**’ values; and ‘01’, ‘10’ are the “idle” ‘**bicast**’ value) for each input signal (For example see col. 18, line 63 through col. 19, line 18) to support grouping channels, e.g. multicasting.

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Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Yang**, by implementing the control circuit and routing tag generator, in assigning different control sequences for the routing tag, into the **Lee**'s controller and arbitrator, with the motivation being to improve the ability to support grouping channels as disclosed in **Yang**: col. 9, lines 15-25.

*Allowable Subject Matter*

9. Claims 9-11 and 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Yang et al.** (U.S.5,987,028), **Park, Jae-Hyun** (U.S.6,563,819), **Chen et al.** (U.S.5,671,222) and **Min et al** ("A Nonblocking Architecture for Broadband Multichannel Switching", IEEE/ACM Transactions on Networking, Vol. 3, No. 2, April 1995, 1063-6692/95, pages 181-198) are all cited to show devices and methods for improving modem communication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (571) 272-3074. The examiner can normally be reached on M-F (8:00-4:30).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on (571) 272-3126.

**Any response to this action should be mailed to:**

**Commissioner of Patents and Trademarks**

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tri H. Phan  
March 31, 2005



**BRIAN NGUYEN**  
**PRIMARY EXAMINER**